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Breaking New Ground: Division Directly in Memory

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***Abstract*—In-memory computing (IMC) has emerged as a promising paradigm for overcoming the limitations of traditional von Neumann architectures by reducing data movement and enhancing computational efficiency. Despite significant advancements in this area, implementing complex arithmetic operations, such as *division*, directly within memory has remained an elusive challenge. This paper introduces a pioneering technique for performing division operations directly in memory, representing the first successful integration of such functionality into the IMC framework. Our approach leverages an innovative circuit based on an unconventional model of computing–*stochastic computing*. Our technique extends the computational capabilities of IMC systems and paves the way for lightweight division operations.**

I. Introduction

By scaling VLSI systems, designers encounter significant challenges, from long operation cycles and complicated circuits to high power consumption and error rates. To tackle these issues, novel technologies such as in-memory computing (IMC) and stochastic computing (SC), coupled with emerging devices such as magnetic tunnel junctions (MTJs) have been proposed [1]. The traditional von Neumann architecture has inherent limitations, including long memory access times, increased leakage power, and reduced performance due to memory bandwidth constraints. Processing-in-memory embeds certain logic structures directly in memory, circumventing the need for the central processor. Fast and efficient in-memory execution of complex arithmetic operations is an ongoing research. To the best of our knowledge, there is no prior work on realizing *division* operation directly in memory. In contrast to the dominant binary radix model, this work utilizes an alternative computing model where data is processed in the form of bit-streams, encoded with the probability of observing a `1`.

This work introduces a pioneering concept: the first in-memory divider utilizing SC and cutting-edge MTJs and FinFET transistors. The resistive nature, random behavior, and radiation hardness of spintronic devices, such as MTJs, have made them particularly beneficial for IMC structures. The power consumption of IMC structures can be significantly decreased by utilizing MTJ devices [2]. MTJs have excellent integration capabilities and can be manufactured independently on top of transistors, making them compatible with various types of transistor technologies.

II. Proposed Approach

Conventional binary division involves a complex process that requires many processing steps. It takes a significant latency and consumes a large chip area for implementation. In contrast, SC division can be simply performed using a multiplexer (`MUX`) unit composed of two `AND` gates and one `OR` gate, as proposed in [3] and shown in Fig. 1(a) where $X1$ and $X2$ are the input stochastic numbers (i.e., bit-streams). The output (Z) gives $X1$ if $X2$ equals `1`, and the last result repeats if $X2$ equals 0. Consider $X1$=1001010000000000 ($P_{X1}=\frac{3}{16}$) and $X2$=1001110000010000 ($P_{X2}=\frac{5}{16}$) as the inputs of the divider; the output is Z=1111011111100000 ($P_Z=\frac{10}{16}=0.625$), which closely approximates the expected output of 0.6. To realize SC division in memory, we implement a `MUX` design that takes advantage of the logic in-memory (LIM) (see Fig. 1(b)) proposed in [4]. This architecture incorporates in-plane anisotropy SHE-MTJ and FinFET transistors to enable logical operations inside the memory.

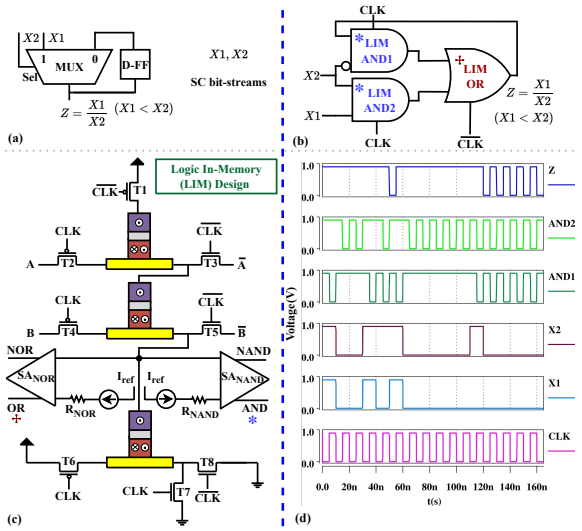

Fig. 1. Divider design: (a) SC circuit [3], (b) Proposed LIM gate-level circuit, (c) Schematic of the magnetic in-memory `AND`/`OR` gate, (d) Timing diagram of the input/output signals.

TABLE I
Accuracy of IMC Division Operation

Bit-stream length, N	16	32	64	128	256	512	1024
Mean Absolute Error(%)	12.51	8.46	6.07	4.24	2.92	2.15	1.61

MAE is measured between the LIM divider *versus* accurate 8-bit binary division.

The design operates in two distinct modes of "*preparation*" and "*evaluation*," depending on the clock signal (`CLK`). During the *preparation* phase (`CLK=0`), the two inputs are stored in MTJs by changing the magnetization of MTJs' free layer. In the *evaluation* phase (`CLK=1`), the sense amplifiers (SA) produce `AND`/`NAND` and `OR`/`NOR` outputs as shown in Fig. 1(c).

In the proposed design, `AND1` and `AND2` function with the `CLK` signal, while `OR1` operates with $\overline{\texttt{CLK}}$. As a result, when `CLK=0`, `OR1` is in the *evaluation* mode, and its output is directed to `AND1`, which is in the *preparation* mode. Conversely, when `CLK=1`, the outputs of `AND1` and `AND2` are evaluated and delivered to the inputs of `OR1`. Compared to [3], our proposed design eliminates the `D`-latch element by using the clock difference technique.

We performed circuit-level simulation using HSPICE, as illustrated in Fig. 1(d), following the simulation setup detailed in [4]. Dividing two N-bit bit-streams using the proposed structure can be completed in $(N+\frac{1}{2})$ cycles. The proposed LIM divider provides accuracy similar to the off-memory CMOS-based SC division. Table I reports the accuracy results for various bit-stream lengths. The proposed divider consumes $8.78\mu W$ of power and $144fJ$ of energy in each cycle. Here, we assumed the inputs are pre-stored in memory in bit-stream format. Future work will involve extending the design with efficient binary-to-bit-stream conversion for seamless arithmetic binary division in memory.

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